

Claims

Sub C3 → 1 1. A circuit for input side impedance matching of a power amplifier in an electronic
2 device, comprising:
3 a source for providing a signal, wherein the signal has a predetermined
4 impedance; and
5 an impedance transformer network joined in parallel with the source, wherein
6 the network comprises a negative resistor in series with an inductor, and wherein the
7 network synthesizes the predetermined impedance at an input of the power
8 amplifier.

1 2. The circuit of claim 1, wherein the inductor has a reactance equal to a capacitance
2 of the device at a required frequency of operation.

3. The circuit of claim 2, wherein the inductor is a bondwire inductor.

1 4. The circuit of claim 1, wherein a value of the negative resistor is selected to
2 synthesize the predetermined impedance at an input of the power amplifier.

1 5. The circuit of claim 4, wherein the value of the negative resistor is approximately
2 -7.4 Ohms.

1 6. The circuit of claim 4, wherein the predetermined impedance is approximately 50
2 Ohms.

1 7. The circuit of claim 4, wherein a normalized phase of the synthesized impedance
2 is between approximately -0.5 to 0.5 Radians.

1 8. The circuit of claim 7, wherein the normalized phase is approximately -0.4
2 Radians.

1 9. The circuit of claim 1, wherein a ratio of signal voltage at an input of the power
2 amplifier to signal voltage at the source is approximately 0.62.

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1 10. A circuit for input side impedance matching of a power amplifier in an electronic
2 device, comprising:
3 a source for providing a signal, wherein the signal has a predetermined
4 impedance;
5 an impedance transformer network joined in parallel with the source, wherein
6 the network comprises a negative resistor in series with an inductor; and
7 wherein a value of the negative resistor is selected to synthesize the
8 predetermined impedance at an input of the power amplifier, and wherein the
9 inductor has a reactance equal to a capacitance of the device at a required frequency
10 of operation.

1 11. The circuit of claim 10, wherein the predetermined impedance is approximately
2 50 Ohms, and wherein the value of the negative resistor is approximately -7.4
3 Ohms.

1 12. The circuit of claim 11, wherein the synthesized impedance has a normalized
2 phase between approximately -0.5 and 0.5 Radians.

1 13. The circuit of claim 12, wherein the normalized phase is approximately -0.41
2 Radians.

- 1 14. The circuit of claim 13, wherein a ratio of signal voltage at the input to signal
2 voltage at the source is approximately 0.62.

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1 15. A method for matching impedance at an input of a power amplifier in an
2 electronic device, comprising the steps of:
3 providing a signal from a source, wherein the provided signal has a
4 predetermined impedance;
5 joining an impedance transformer network in parallel with the source,
6 wherein the network comprises a negative resistor in series with an inductor; and
7 selecting a value for the negative resistor so that the predetermined
8 impedance is synthesized at the input of the power amplifier.

1 16. The method of claim 15, further comprising the step of setting a reactance of the
2 inductor equal to a capacitance of the device at a required frequency of operation.

1 17. The method of claim 15, wherein the selecting step comprises selecting a value
2 of -7.4 Ohms for the negative resistor.

1 18. The method of claim 15, wherein the predetermined impedance is approximately
2 50 Ohms.

1 19. The method of claim 15, wherein a normalized phase of the synthesized
2 impedance is approximately -0.41 Radians.

- 1 20. The method of claim 15, wherein a ratio of signal voltage at the input to signal
- 2 voltage at the source is approximately 0.62.

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